CLAIMS

What is claimed is:

1. A magnetoresistive random access memory (MRAM) unit comprising:

a substrate;

a plurality of transistors formed on said substrate, each of said plurality of transistors being a field-effect transistor comprising a first source/drain electrode, a second source/drain electrode and a gate electrode;

a plurality of active areas defined in a common memory block comprising a ferromagnetic recording layer, a free magnetic reading layer, a non-magnetic space layer between said ferromagnetic recording layer and said free magnetic reading layer~~, and a plurality of active areas defined in said common memory block~~;

a plurality of contacts, each of said plurality of contacts electrically connecting a respective one of said first source/drain electrodes with a corresponding one of said plurality of active areas; and

a common electrode in electrical contact with said plurality of contacts through said common memory block, said common electrode serving as bit line for said first source/drain electrodes;

wherein each of said plurality of active areas forms an effective magnetoresistive element; and

wherein each of said plurality of transistors is controllable to electrically activate a corresponding one of said plurality of contacts and thereby to write/read a data bit into/from said ferromagnetic recording layer at a respective one of said effective magnetoresistive elements.

2. The MRAM unit as claimed in claim 1, wherein said corresponding one of said plurality of contacts is electrically activatable by means of electrically connecting said respective one of said first source/drain electrodes with said corresponding second source/drain electrode.

3. The MRAM unit as claimed in claim 1, wherein a plurality of bit lines is in electrical contact with said second source/drain electrodes.

4. The MRAM unit as claimed in claim 1, wherein a plurality of word lines is in electrical contact with said gate electrodes.

5. The MRAM unit as claimed in claim 1, wherein a common auxiliary electrode is provided in electrical contact between said common electrode and said common memory block.

6. The MRAM unit as claimed in claim 1, wherein a common digital line is provided next to said common electrode on an opposite side of said common electrode with respect to said common memory block.

7. The MRAM unit as claimed in claim 6, wherein said common digital line is electrically insulated from said common electrode.

8. The MRAM unit as claimed in claim 1, wherein said ferromagnetic recording layer is provided between said common electrode and said non-magnetic space layer.

9. The MRAM unit as claimed in claim 1, wherein an electrically insulating confinement layer comprising a plurality of openings corresponding to said plurality of contacts is provided between said common memory block and said plurality of contacts.

10. The MRAM unit as claimed in claim 1, wherein said ferromagnetic recording layer is a synthetic antiferromagnetic pinned multi-layer comprising at least two antiferromagnetically coupled ferromagnetic layers pinned by an antiferromagnetic (AFM) layer.

11. The MRAM unit as claimed in claim 1, wherein said ferromagnetic recording layer is a hard magnetic layer.

12. The MRAM unit as claimed in claim 1, wherein said ferromagnetic recording layer is a ferromagnetic layer coupled with a hard magnetic layer.

13. The MRAM unit as claimed in claim 1, wherein said common memory block further comprises a template layer next to said plurality of contacts and a cap layer next to said common electrode.

14. The MRAM unit as claimed in claim 13, wherein at least one of said template layer, said cap layer and said free magnetic layer is a multi-synthetic ferrimagnetic layer.

15. The MRAM unit as claimed in claim 1, wherein said plurality of contacts is arranged in form of an array.

16. The MRAM unit as claimed in claim 6, wherein said common digital line is adapted to cause a magnetic field in said ferromagnetic recording layer at an activated one of said effective magnetoresistive elements upon a current passing through said common digital line.

17. The MRAM unit as claimed in claim 1, further comprising in each case a heat element adjacent to each effective magnetoresistive element.

18. The MRAM unit as claimed in claim 1, wherein said common memory block is a stacked current-perpendicular-to-plane (CPP) structure such as a magnetic tunnel junction (MTJ) or a CPP spin-valve (SV).

19. A method of writing data in a MRAM unit which comprises a plurality of transistors on a substrate, each of said plurality of transistors being a field-effect transistor and comprising first and second source/drain electrodes and a gate electrode, a plurality of active areas defined in a common memory block which is electrically connected to each of said first source/drain electrodes through in each case one of a plurality of contacts, a common electrode electrically contacting said plurality of contacts through said common memory block, and a common digital line provided electrically isolated next to said common electrode on an opposite side of said common electrode with respect to said common memory block, said

common memory block comprising a ferromagnetic recording layer, a free magnetic reading layer, a non-magnetic space layer between said ferromagnetic recording layer and said free magnetic reading layer ~~and a plurality of active areas defined in said common memory block~~, said method comprising:

controlling said plurality of transistors for electrically activating a corresponding one of said plurality of contacts, thereby electrically activating a respective active area of said plurality of active areas, said activated respective active area serving as effective magnetoresistive element;

raising the temperature of said ferromagnetic recording layer at said effective magnetoresistive element to approach or exceed its critical temperature independently of other active areas, thereby reducing the coercitivity of said ferromagnetic recording layer at said effective magnetoresistive element; and

writing a magnetization state representing a bit of said data in said ferromagnetic recording layer at said effective magnetoresistive element by passing a current through said common digital line.

20. The method according to claim 19, further comprising cooling down said ferromagnetic recording layer at said effective magnetoresistive element to nearly ambient temperature after writing said magnetization state in said ferromagnetic recording layer at said effective magnetoresistive element.

21. The method according to claim 19, wherein raising the temperature of said ferromagnetic recording layer at said effective magnetoresistive element to above its critical temperature independently of other active areas further comprises passing a heating current partly through said common electrode, completely through said effective magnetoresistive element, completely through said activated corresponding one of said plurality of contacts and completely through said controlled one of said plurality of transistors via said corresponding first and second source/drain electrodes.

22. The method according to claim 21, further comprising passing said heating current through a heat element being thermally coupled to said effective magnetoresistive element.

23. The method according to claim 21, further comprising electrically confining said heating current by means of providing an electrically insulating confinement layer comprising a plurality of openings corresponding to said plurality of contacts between said common memory block and said plurality of contacts.

24. The method according to claim 19, wherein controlling said plurality of transistors comprises applying a control voltage to said gate electrode of a respective one of said plurality of transistors and applying a voltage difference to said first and second source/drain electrodes of said respective one of said plurality of transistors.

25. A method of performing a read operation in a MRAM unit which comprises a plurality of transistors on a substrate, each of said plurality of transistors being a field-effect transistor and comprising first and second source/drain electrodes and a gate electrode, a plurality of active areas defined in a common memory block which is electrically connected to each of said first source/drain electrodes through in each case one of a plurality of contacts, a common electrode electrically contacting said plurality of contacts through said common memory block, and a common digital line provided electrically isolated next to said common electrode on an opposite side of said common electrode with respect to said common memory block, said common memory block comprising a ferromagnetic recording layer, a free magnetic reading layer, a non-magnetic space layer between said ferromagnetic recording layer and said free magnetic reading layer ~~and a plurality of active areas defined in said common memory block,~~ said method comprising:

controlling said plurality of transistors for electrically activating a corresponding one of said plurality of contacts, thereby electrically activating a respective active area of said plurality of active areas, said activated respective active area serving as effective magnetoresistive element;

applying a current through said common digital line, thereby adjusting all magnetization states in said free magnetic reading layer; and

determining the magnetization state of said ferromagnetic recording layer at said effective magnetoresistive element, wherein the resistance states of said

ferromagnetic recording layer at said effective magnetoresistive element are dependent on the relative angles between the magnetization vectors of said ferromagnetic recording layer at said effective magnetoresistive element and of said free magnetic reading layer.

26. The method according to claim 25, wherein controlling said plurality of transistors comprises applying a control voltage to said gate electrode of a respective one of said plurality of transistors and applying a voltage difference to said first and second source/drain electrodes of said respective one of said plurality of transistors.